USB3-PCIEv2 project PCB tech specification.

Overall PCB dimension: 83.5 x 33 mm ±0.2 mm

Overall PCB thickness: 1.17 mm ±10%

Minimal trace width/gap: 6/6 mil (0.15/0.15 mm)

Minimal VIA size/hole: 24/12mil (0.6/0.3 mm)

Minimal hole/hole clearance: 12mil (0.3 mm)

Minimal pad-to-pad clearance (solder mask might be omitted): 6 mil (0.15 mm)

Material: FR4 TG150-160 or similar

Finished outer copper: 1 oz (0.035 mm)

Finished inner copper: 1 oz (0.035 mm)

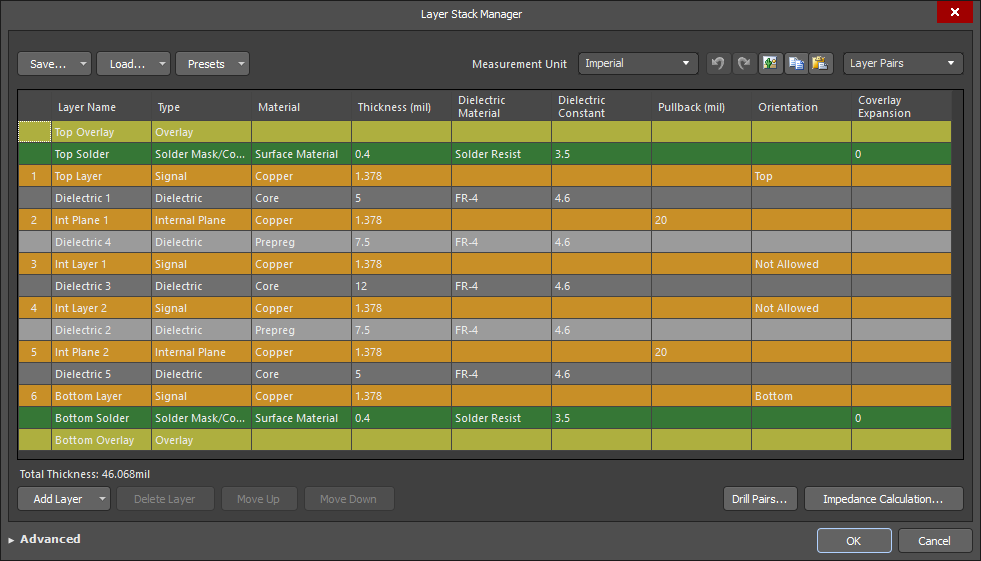
Finishing: Immersion Gold

Solder Mask color: Green

Silkscreen: White

Other: Vendor to mark its logo, date code, test pass, etc. - allowed on bottom mask or silkscreen.

Preferable 6 layers stack-up (for example):



Use the next lines options to simulate real stack-up for proper impedance:

USB lane diff pair impedance: 90 Ohm ±10%, inner trace 6 mil (0.1524 mm), gap 8 mil (0.2032 mm)

PCIe lane diff pair impedance: 100 Ohm ±10%, inner trace 5.906 mil (0.15 mm), gap 10.8 mil (0.2743 mm)

Gerber files definitions:

Overlay (Silk) Top - USB3-PCIEv2.GTO

Solder (Mask) Top - USB3-PCIEv2.GTS

L1: Top Layer - USB3-PCIEv2.GTL

L2: Int Plane 1 - USB3-PCIEv2.GP1 (Negative Plain)

L3: Int Layer 1 - USB3-PCIEv2.G1

L4: Int Layer 2 - USB3-PCIEv2.G2

L5: Int Plane 2 - USB3-PCIEv2.GP2 (Negative Plain)

L6: Bottom Layer - USB3-PCIEv2.GBL

Solder (Mask) Bottom - USB3-PCIEv2.GBS

Overlay (Silk) Bottom - USB3-PCIEv2.GBO

Drilling/milling layers:

KeepOut (Border) - USB3-PCIEv2.GKO

NC drill plated Top to Bottom - USB3-PCIEv2-Plated.TXT

NC drill non-plated Top to Bottom - USB3-PCIEv2-NonPlated.TXT

Stencil layers:

Paste Top - USB3-PCIEv2.GTP

Paste Bottom – USB3-PCIEv2.GBP

Assembly layers:

Mechanical Top - USB3-PCIEv2.GM1

Mechanical Bottom – USB3-PCIEv2.GM2